

Appl. No. 10/603,361
Reply to Office Action of 06/29/2006
Amdt. dated 09/26/2006

RECEIVED Docket No.: N1085-00089
CENTRAL FAX CENTER TSMC 2002-0917

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Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

- 1 1. (Currently Amended) A method of making a multiple gate electrode on a semiconductor device, comprising the steps of:
 - 3 coating a layer of gate electrode material over top and past the opposed sides of
 - 4 a semiconductor device that has been previously coated with a thin film of gate
 - 5 dielectric on the top and the opposed sides of the semiconductor device; and
 - 6 planarizing the layer of gate electrode material to produce a substantially planar
 - 7 surface formed only of the gate electrode material disposed atop the semiconductor
 - 8 device and extending distally past each of the opposed sides, prior to patterning the
 - 9 gate electrode material to form a discrete multiple gate electrode on the semiconductor
 - 10 device, the substantially planar surface having the same height at locations superjacent
 - 11 the semiconductor device and at locations distal the semiconductor device.
- 1 2. (Currently Amended) The method of claim 1, further comprising the steps of:
 - 2 applying a photoresist mask of substantially uniform thickness and a planar top
 - 3 surface on the planar top surface of the planarized gate electrode material including
 - 4 directly over the semiconductor device;
 - 5 patterning the photoresist mask to cover a corresponding pattern of the discrete
 - 6 multiple gate electrode; and
 - 7 etching the gate electrode material that is uncovered by the photoresist mask to
 - 8 form the discrete multiple gate electrode.
- 1 3. (Original) The method of Claim 1, further comprising the step of:

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2 conforming the layer of gate electrode material with a step height increase
3 corresponding to an increased step height of the semiconductor device.

1 4. (Original) The method of claim 1, wherein the semiconductor device
2 comprises a silicon fin

1 5. (Original) The method of claim 1 wherein, the semiconductor device comprises a
2 fin of silicon and germanium.

1 6. (Currently Amended) The method of claim 1, further comprising the steps of:

2 applying a photoresist mask of substantially uniform thickness and a planar top
3 surface on the planar top surface of the planarized gate electrode material including
4 directly over the semiconductor device, the mask comprising photoresist and a mask
5 material selected from the group comprising, silicon nitride, silicon oxynitride, silicon
6 oxide and photo resist, or combinations thereof;

7 patterning the photoresist mask to cover a corresponding pattern of the multiple
8 gate electrode; and

9 etching the gate electrode material that is uncovered by the photoresist mask to
10 form the discrete multiple gate electrode.

1 7. (Currently Amended) The method of claim 1, further comprising the steps of:

2 applying a photoresist mask of substantially uniform thickness and a planar top
3 surface on the planar top surface of the planarized gate electrode material including
4 directly over the semiconductor device;

5 patterning the photoresist mask to cover a corresponding pattern of the multiple
6 gate electrode; and

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7 plasma etching the gate electrode material that is uncovered by the photoresist
8 mask to form the patterned multiple gate electrode.

1 8. (Original) The method as recited in claim 1, further comprising the step of:
2 applying a mask over the planarized surface, wherein the mask is of substantially
3 uniform thickness for accurate patterning thereof.

1 9. (Original) The method of claim 1 wherein, the gate dielectric comprises silicon
2 oxide.

1 10. (Original) The method of claim 1 wherein, the gate dielectric comprises silicon
2 oxynitride.

1 11. (Original) The method of claim 1 wherein, the gate dielectric comprises a high
2 permittivity material.

1 12. (Original) The method of claim 1 wherein, the gate dielectric comprises a material
2 having a permittivity greater than 5.

1 13. (Original) The method of claim 1 wherein, the gate dielectric comprises a
2 thickness in the range of 3 and 100 Angstroms.

1 14. (Original) The method of claim 1 wherein, the multiple gate electrode comprises
2 polycrystalline silicon.

1 15. (Original) The method of claim 1 wherein, the multiple gate electrode comprises
2 a conductive material.

1 16. (Original) The method of claim 1 wherein, the multiple gate electrode comprises
2 a metal material.

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1 17. (Currently Amended) A semiconductor device having a multiple gate electrode,
2 comprising:

3 the semiconductor device having a projecting fin coated with a gate dielectric film
4 over top and opposed sides of the fin;

5 a multiple gate electrode on each of the opposed sides of the fin, the multiple
6 gate electrode formed of a layer of gate electrode material and having a substantially
7 planar surface disposed atop the gate dielectric film formed over the top of the fin and
8 extending distally past each of the opposed sides of the fin; and

9 a patterned mask on the planar surface of the multiple gate electrode, the
10 patterned mask having a substantially uniform thickness and a substantially planar
11 surface including over the fin.

1 18. (Previously Presented) The semiconductor device of claim 17 wherein, the
2 multiple gate electrode is a portion of the layer of gate electrode material which has a
3 planarized surface that includes the planar surface of the multiple gate electrode.

1 19. (Cancelled)